Low Noise, Low Input Bias Current, Rail-to-Rail Output, JFET Dual Operational Amplifier

Data Sheet

ADA4001-2

FEATURES

- Low T_CV_{OS}: ±5 µV/°C typical
- Low input bias current: 20 pA typical at V_{SY} = ±15 V
- Low noise
  - 7.7 nV/√Hz typical at f = 1 kHz
  - 1.2 µV rms at 20 Hz to 20 kHz
- Low distortion: 0.00006%
- No phase reversal
- Rail-to-rail output
- Unity-gain stable

APPLICATIONS

- Instrumentation
- Medical instruments
- Multipole filters
- Precision current measurement
- Photodiode amplifiers
- Sensors
- Audio

PIN CONFIGURATION

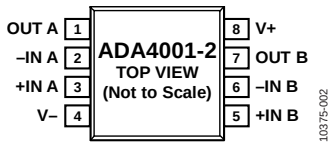

Figure 1. 8-Lead SOIC_N (R Suffix)

GENERAL DESCRIPTION

The ADA4001-2 is a dual channel JFET amplifier that features low input voltage noise and current noise, input bias current, and rail-to-rail output.

The combination of low noise and low input bias current makes this amplifier especially suitable for high impedance sensor amplification. With low noise and fast settling times, the ADA4001-2 provides good accuracy for medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the ADA4001-2 maintains fast settling performance even with substantial capacitive loads, and, unlike many older JFET amplifiers, the ADA4001-2 does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

With fast slew rate and great stability under capacitive loads, the ADA4001-2 is a good fit for filter applications. With low input bias currents and noise, it offers a wide dynamic range for photodiode amplifier circuits. Low noise and distortion, along with high output current and excellent speed, make the ADA4001-2 a great choice for audio applications.

The ADA4001-2 is specified over the −40°C to +125°C extended industrial temperature range.

The ADA4001-2 is available in an 8-lead narrow SOIC package.

Rev. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

5/12—Rev. A to Rev B

Changes to General Description Section 1
Changed Input Impedance to Input Capacitance Throughout .. 3
Added Input Resistance Parameter, Table 1 3
Change to Figure 5 Caption 5

2/12—Rev. 0 to Rev. A

Changes to Figure 27 9

2/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{SY} = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			±0.5	±1.5	mV
		−40°C < T_A < +125°C			±2.5	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			±5		µV/°C
Input Bias Current	I_B			20	30	pA
		−40°C < T_A < +125°C			4	nA
Input Offset Current	I_{OS}				20	pA
		−40°C < T_A < +125°C			2	nA
Input Voltage Range			−12.5		+12.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −12.5 V to +12.5 V	96	105		dB
		−40°C < T_A < +125°C	90			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = −13.5 V to +13.5 V	104	112		dB
		R_L = 2 kΩ, V_O = −13.5 V to +13.5 V	104	112		dB
		−40°C < T_A < +125°C	90			dB
		R_L = 600 Ω, V_O = −13.0 V to +13.0 V	90	93		dB
Input Capacitance, Differential	C_{DM}	V_{CM} = 0 V		3.1		pF
Input Capacitance, Common-Mode	C_{CM}	V_{CM} = 0 V		4.8		pF
Input Resistance		V_{CM} = 0 V		$>1 \times 10^{13}$		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ	14.8			V
		R_L = 2 kΩ	14.5			V
		R_L = 600 Ω	13.5			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ			−14.8	V
		R_L = 2 kΩ			−14.5	V
		R_L = 600 Ω			−13.5	V
Short-Circuit Current	I_{SC}			±50		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	96	110		dB
		−40°C < T_A < +125°C	93			dB
Operating Voltage Range			±5		±18	V
Supply Current/Amplifier	I_{SY}	V_O = 0 V		2	3	mA
					4	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	±15[1]	±25		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 100		16.7		MHz
Unity-Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = 1		10.2		MHz
Phase Margin	φ_M			76		Degrees
−3 dB Closed-Loop Bandwidth	−3 dB	A_V = 1, V_{IN} = 5 mV p-p		10.3		MHz
Settling Time	t_S	To 0.01%, 10 V step, G = +1		1.2		µs
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, G = +1, R_L = 2 kΩ		0.00006		%
NOISE PERFORMANCE						
Voltage Noise	e_n rms	20 Hz to 20 kHz		1.2		µV rms
Voltage Noise Density	e_n	f = 100 Hz		8.8		nV/√Hz
		f = 1 kHz		7.7		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		3		fA/√Hz

[1] Guaranteed by design and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	3000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3.

Package Type	θ_{JA} [1]	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	130	45	°C/W

[1] θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

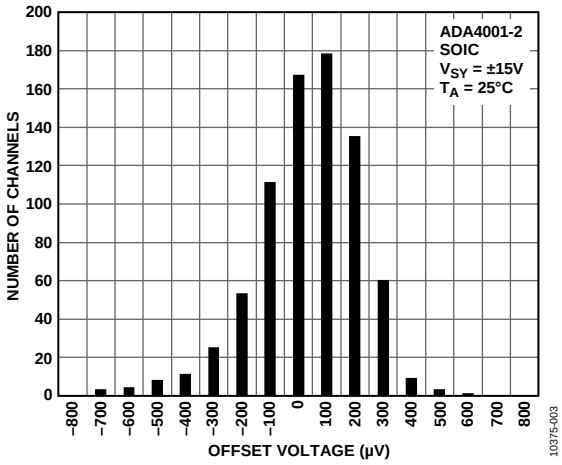

Figure 2. Input Offset Voltage Distribution

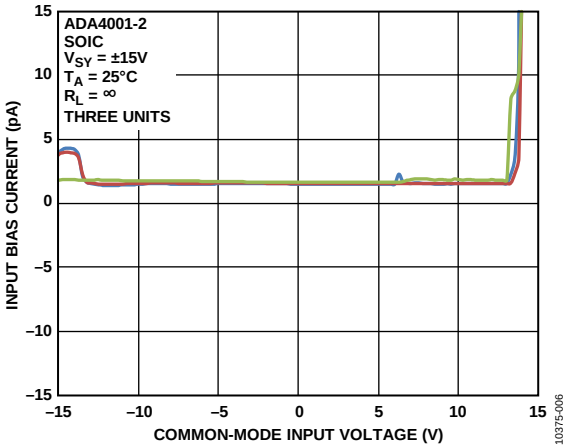

Figure 5. Input Bias Current vs. Common-Mode Voltage

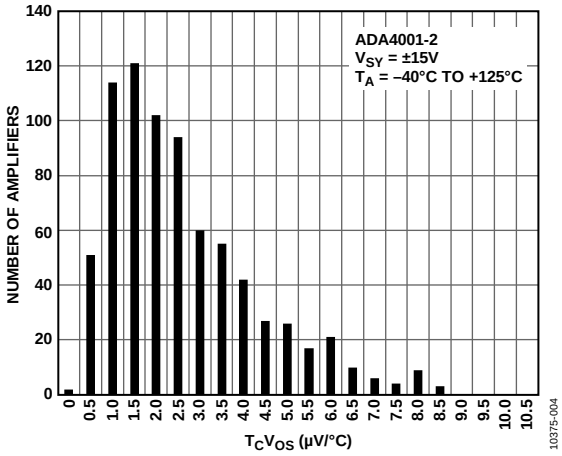

Figure 3. T_CV_{OS} Distribution

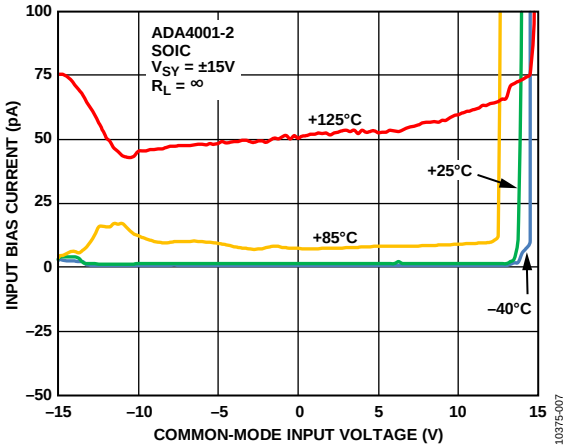

Figure 6. Input Bias Current vs. V_{CM} and Temperature

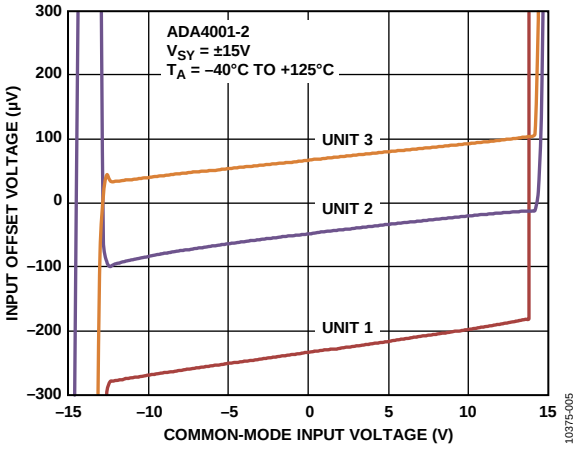

Figure 4. Input Offset Voltage vs. Common-Mode Voltage

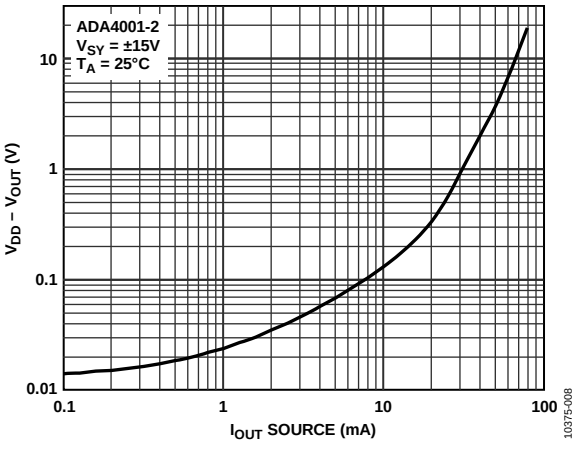

Figure 7. Dropout Voltage vs. Source Current

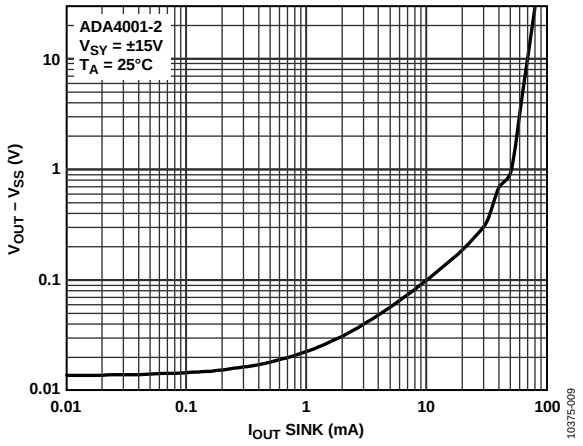

Figure 8. Dropout Voltage vs. Sink Current

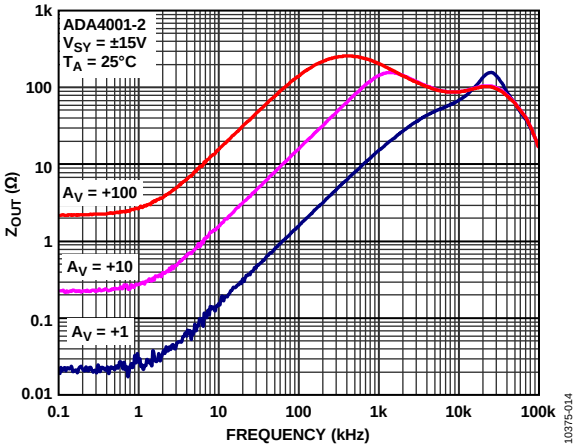

Figure 11. Closed-Loop Output Impedance vs. Frequency

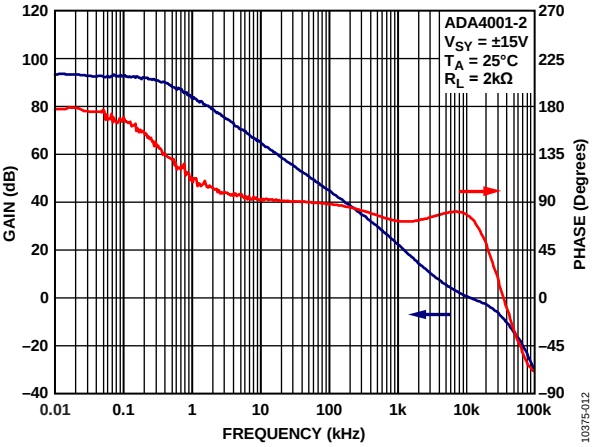

Figure 9. Open-Loop Gain and Phase vs. Frequency

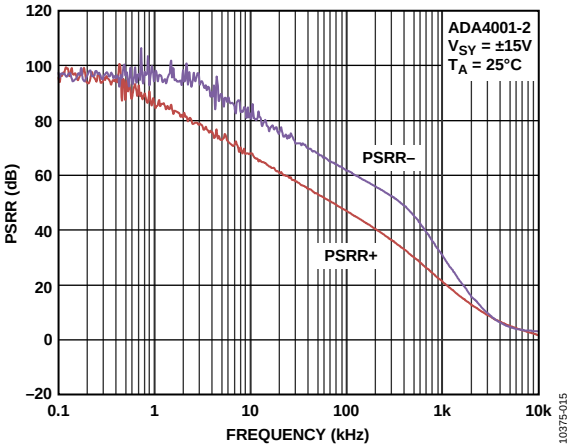

Figure 12. PSRR vs. Frequency

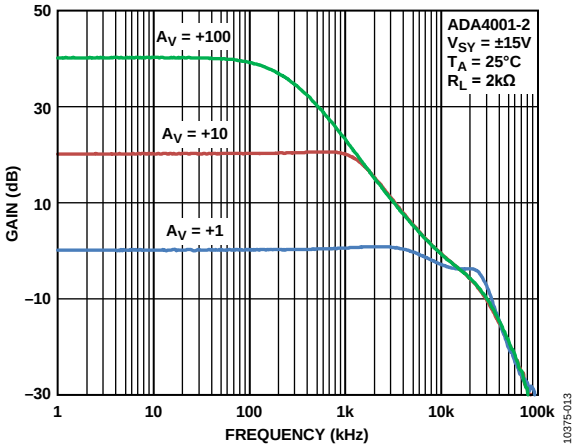

Figure 10. Closed-Loop Gain vs. Frequency

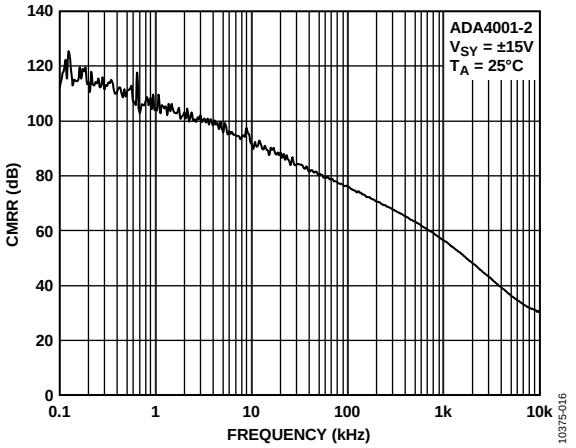

Figure 13. CMRR vs. Frequency

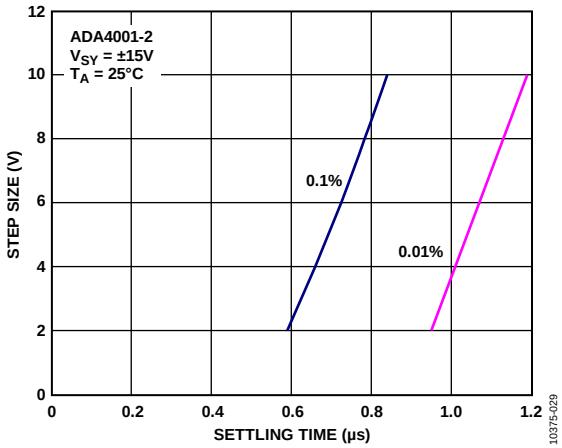

Figure 14. Settling Time Positive Step

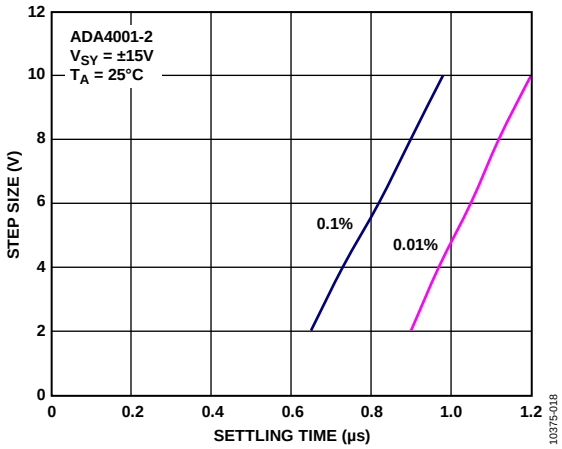

Figure 17. Settling Time Negative Step

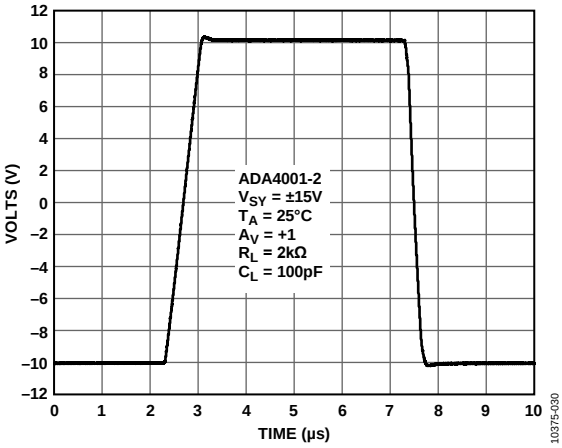

Figure 15. Large Signal Transient Response

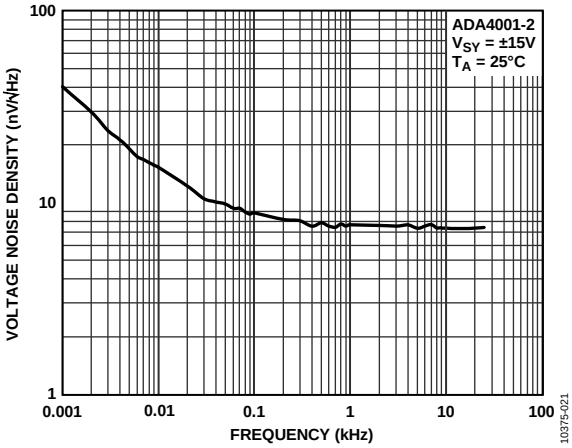

Figure 18. Voltage Noise Density

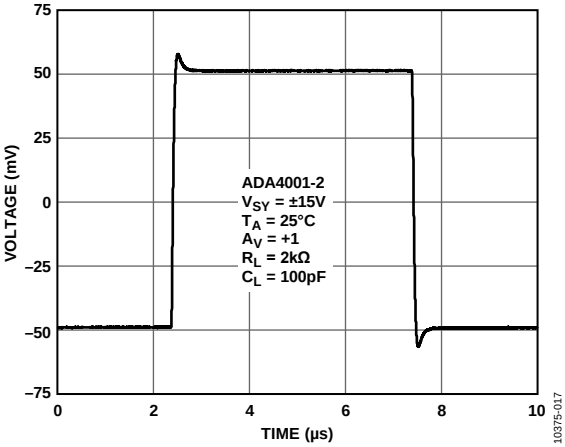

Figure 16. Small Signal Transient Response

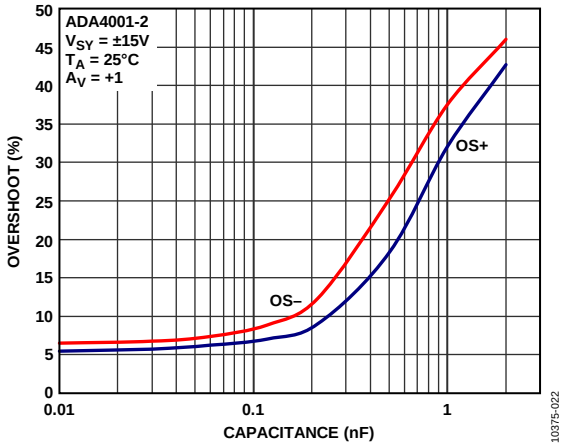

Figure 19. Overshoot vs. Load Capacitance

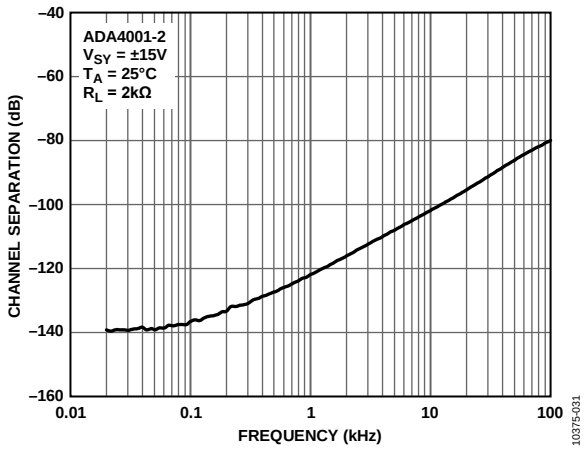

Figure 20. Channel Separation

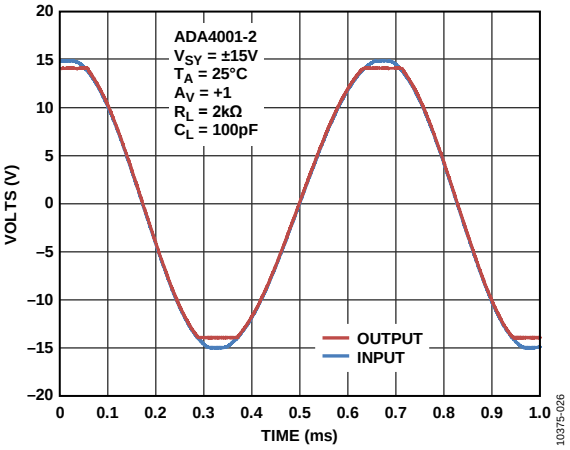

Figure 23. No Phase Reversal

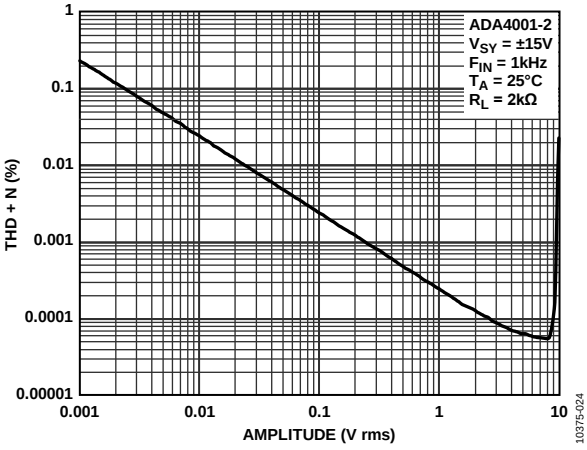

Figure 21. THD + N vs. Amplitude

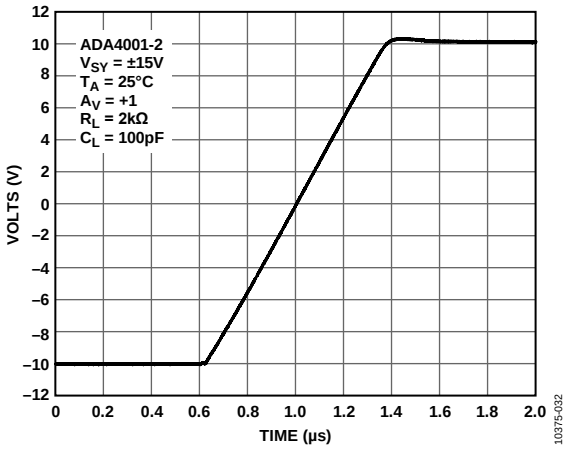

Figure 24. Positive Slew Rate

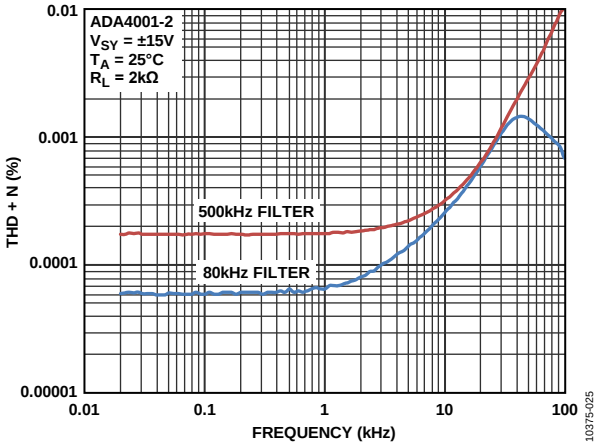

Figure 22. THD + N vs. Frequency

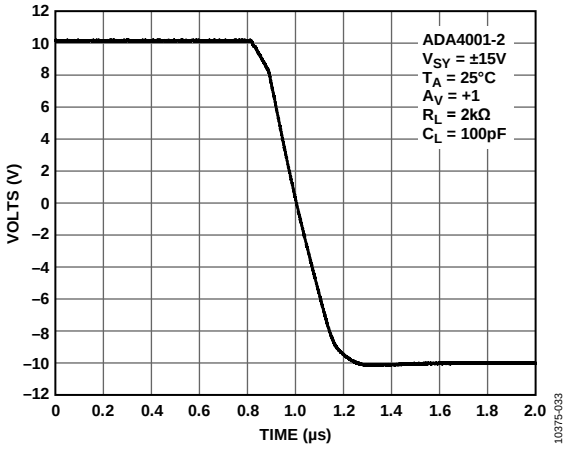

Figure 25. Negative Slew Rate

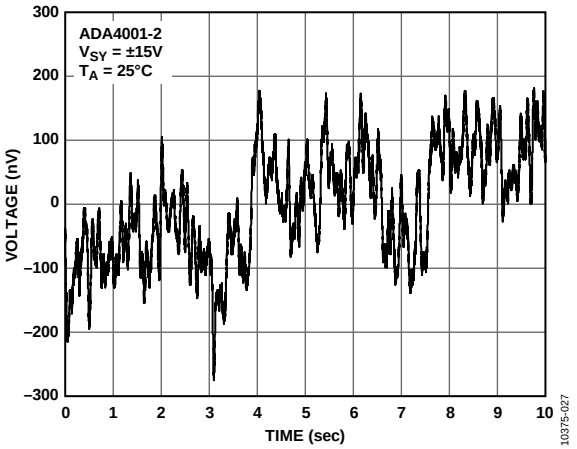

Figure 26. Peak-to-Peak Voltage Noise

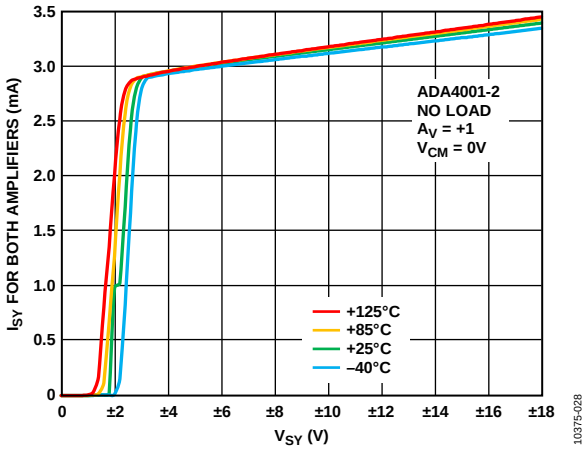

Figure 27. Supply Current vs. Supply Voltage and Temperature

APPLICATIONS INFORMATION

TOTAL NOISE INCLUDING SOURCE RESISTORS

The low input current noise and input bias current of the ADA4001-2 makes it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature. The total noise density of the circuit is

$$e_{nTOTAL} = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S}$$

where:
e_n is the input voltage noise density of the part.
i_n is the input current noise density of the part.
R_S is the source resistance at the noninverting terminal.
k is Boltzmann's constant (1.38×10^{-23} J/K).
T is the ambient temperature in Kelvin (T = 273 + °C).

For $R_S < 4$ kΩ, e_n dominates and $e_{nTOTAL} \approx e_n$. The current noise of the ADA4001-2 is so low that its total density does not become a significant term unless R_S is greater than 100 MΩ, an impractical value for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as

$$e_{nTOTAL} = e_{nTOTAL}\sqrt{BW}$$

where BW is the bandwidth in hertz.

Note that the previous analysis is valid for frequencies larger than 150 Hz and assumes flat noise above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

I-V CONVERSION APPLICATIONS

Photodiode Circuits

Common applications for I-V conversion include photodiode circuits where the amplifier is used to convert a current emitted by a diode placed at the positive input terminal into an output voltage.

The ADA4001-2 low input bias current, wide bandwidth, and low noise makes it an excellent choice for various photodiode applications, including fax machines, fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 28 uses a silicon diode with zero bias voltage. This is known as a photovoltaic mode; this configuration limits the overall noise and is suitable for instrumentation applications.

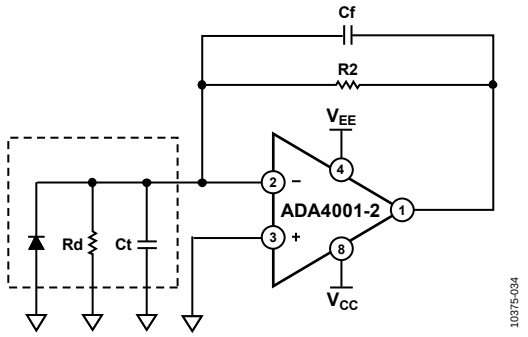

Figure 28. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input capacitance (Ct) consists of the sum of the diode capacitance and the amplifier's input capacitance (8 pF), which includes external parasitic capacitance. Ct creates a pole in the frequency response that can lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 28. It creates a zero and yields a bandwidth whose corner frequency is 1/(2π(R2Cf)).

The value of R2 can be determined by the ratio

$$V/I_D$$

where:
V is the desired output voltage of the op amp.
I_D is the diode current.

For example, if I_D is 100 μA and a 10 V output voltage is desired, R2 should be 100 kΩ. Rd (see Figure 28) is a junction resistance that drops typically by a factor of 2 for every 10°C increase in temperature.

A typical value for Rd is 1000 MΩ. Because Rd >> R2, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is

$$f_{MAX} = \sqrt{\frac{ft}{2\pi R2Ct}}$$

where ft is the unity gain frequency of the amplifier.

Cf can be calculated by

$$Cf = \sqrt{\frac{Ct}{2\pi R2\,ft}}$$

where ft is the unity gain frequency of the op amp, and it achieves a phase margin, φ_M, of approximately 45°.

A higher phase margin can be obtained by increasing the value of Cf. Setting Cf to twice the previous value yields approximately $\varphi_M = 65°$ and a maximal flat frequency response, but it reduces the maximum signal bandwidth by 50%.

INPUT BIAS CURRENT

Because the ADA4001-2 has a JFET input stage, the input bias current, due to the reverse-biased junction, has a leakage current that approximately doubles every 10°C. The power dissipation of the part, combined with the thermal resistance of the package, results in the junction temperature increasing 30°C above ambient. This parameter is tested with high speed ATE equipment, which does not result in the die temperature reaching equilibrium. This is correlated with bench measurements to match the guaranteed maximum at room temperature in Table 1.

The input current can be reduced by keeping the temperature as low as possible and using a light load on the output.

NOISE CONSIDERATIONS

The JFET input stage offers very low input voltage noise and input current noise. The thermal noise of a 1 kΩ resistor at room temperature is 4 nV/√Hz, thus low values of resistance should be used for dc-coupled inverting and noninverting amplifier configurations. In the case of transimpedance amplifiers (TIAs), current noise is more important.

The ADA4001-2 is an excellent choice for both of these applications. Analog Devices, Inc., offers a wide variety of low voltage noise and low current noise op amps in a variety of processes optimized for different supply voltage ranges. Refer to the AN-940 Application Note for a complete discussion of noise, calculations, and selection tables for more than three dozen low noise, op amp families.

OUTLINE DIMENSIONS

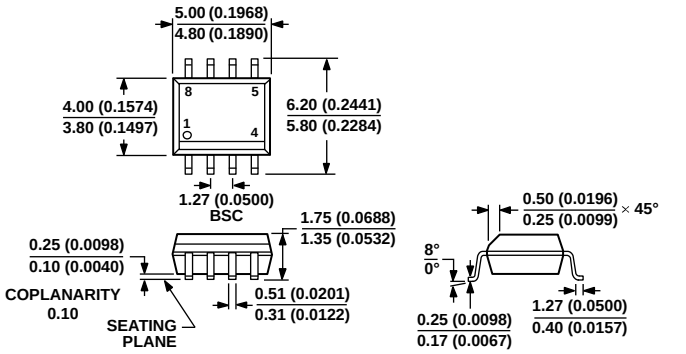

Figure 29. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4001-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8
ADA4001-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8
ADA4001-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.